

# Technology Development of a Compact Radar Digital Receiver

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**Abstract**— As part of a NASA ESTO funded Instrument Incubator Program (IIP), a Ka-band radar interferometer is currently under development to demonstrate the potential for an ice-surface topography, swath-mapping sensor at transmit powers that are technologically feasible and practical. The proposed system utilizes digital beam forming (DBF) with an antenna array in elevation. Each array element utilizes a dedicated receiver (16 receivers in the nominal design). These receivers operate in unison to sample the down-converted, L-band radar returns. The design and implementation of this L-band digital receiver is the focus of this paper.

The digital receivers are compact and flexible to meet the demands of the proposed DBF system, but are designed in a flexible manner such that they could easily be adapted for use in alternate applications. The receiver design is capable of bandpass sampling RF inputs up to 3.3 GHz at 10 bits. An onboard FPGA is utilized for timing and control, but an oversized part was selected to enable the implementation of various application-specific, real-time algorithms. Data are extracted from the receivers via a front-panel data port (FPDP). This data bus interface facilitates low overhead, high data rate and multi-channel functionality. Finally, all of the key components were selected with a spaceborne implementation in mind; they are all available in radiation-hardened equivalents.

## I. BACKGROUND

The estimation of the mass balance of ice sheets and glaciers on Earth is a problem of considerable scientific and societal importance. A key measurement to understanding, monitoring and forecasting these changes is ice-surface topography, both for ice-sheet and glacial regions. Current observations of ice-surface topography are limited in spatial extent and undersampled regions of interest, most particularly the complex and dynamic glacial zones. A Ka-band single-pass interferometric synthetic aperture radar (InSAR) is ideally suited for glacier and ice-sheet mapping [1]. Single-pass imaging radar interferometry has unique capabilities for providing fine resolution, topographic mapping over a wide swath independent of solar illumination. A Ka-band (35-GHz) center frequency maximizes the single-pass interferometric accuracy (proportional to the wavelength), reduces snow penetration (when compared with lower frequencies), and remains relatively impervious to atmospheric attenuation.

Such an instrument, however, is technologically challenging on several fronts. Most notably, previous attempts at using millimeter-wave InSAR faced fundamental

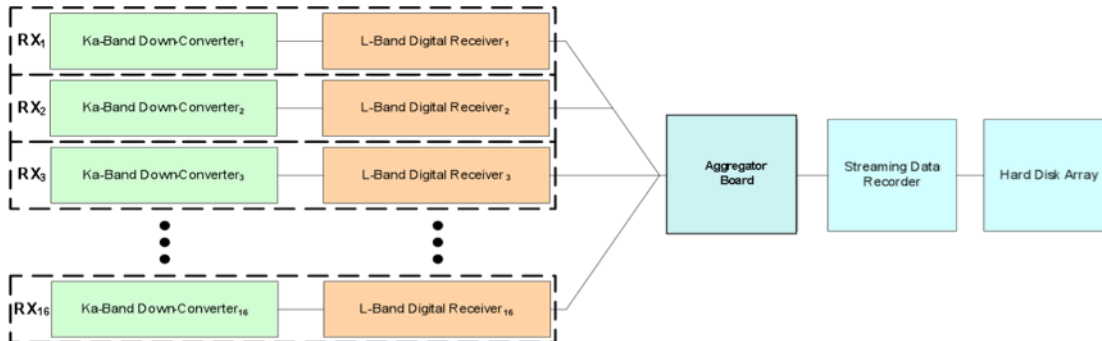


Figure 1: GLISTIN Demonstration System Block Diagram

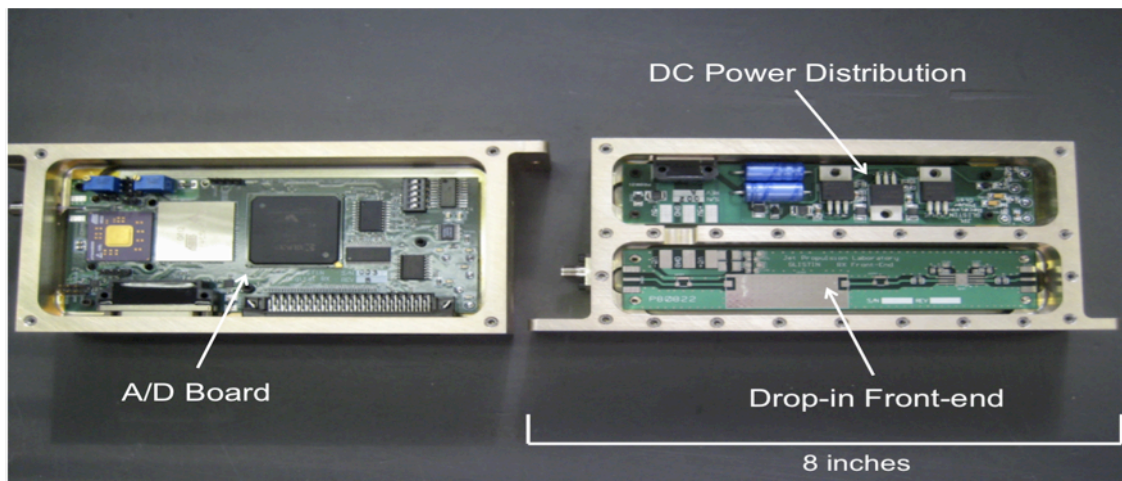


Figure 2: Front & Back Side of Demonstration Receiver in Housing

problems including limited swath widths and high transmitted power requirements. Our approach overcomes those two major limitations by applying digital beamforming (DBF) techniques in elevation to standard InSAR. The result of doing so is over an order of magnitude savings in the peak transmit power requirement, making the solution technologically feasible. As part of the Glacier and Land Ice Surface Topography Interferometer (GLISTIN) instrument incubator program (IIP), we have built a  $\frac{1}{4}$  scale (1m x 1m) Ka-band slotted waveguide antenna comprising 16 elements in elevation [1,2]. A key consequence of employing DBF, however, is an increased data-rate and more complex data-handling requirements since each element in the beamforming array requires a dedicated receiver. It is that receiver design – its networking and implementation – that is the topic of this paper.

## II. RECEIVER ARCHITECTURE

Each receive element in the demonstration instrument consists of a Ka- to L-band down-converter and an L-band digital receiver (see Figure 1). The down-converters were a procured item, while the digital receiver presented one of the major hurdles in the development of the GLISTIN instrument. Currently available digital receivers are large, most are incapable of directly accepting an L-band input and even fewer have a clear path to space-flight readiness. The goal in the design of the GLISTIN digital receiver was to create a flexible, compact receiver capable of

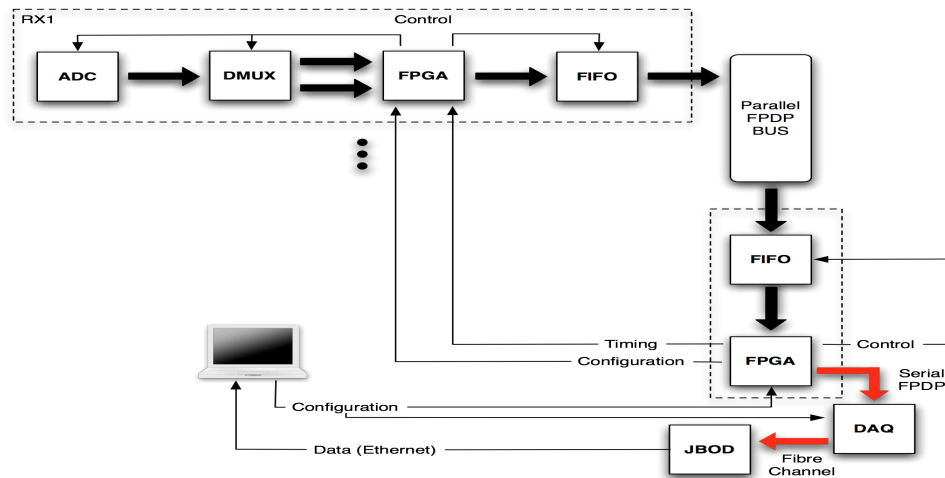
mounting directly to an antenna. In addition to the aforementioned capabilities, the receiver would meet the specific requirements of the GLISTIN instrument while maintaining an open architecture that would enable adapting the receiver to a host of other radar applications with relative ease. A sampling of some of the key GLISTIN requirements is listed in Table 1.

TABLE 1: KEY RECEIVER REQUIREMENTS

Parameters	Requirement	
	Flight	Demo
Bandwidth	40 MHz	80 MHz
Rx Window	178 usec	50 usec
PRF	4 kHz	500 Hz
Noise Figure	4.5 dB	4.5 dB
ENOB	> 7 bits	> 7 bits
ADC Jitter	< 0.01 nsec	< 0.01 nsec

It should be noted that while some of the demonstration and space flight requirements differ, these modifications were made due to the different timing solutions of the ground-based measurements.

Figure 2 depicts the three subassemblies that make up a single digital receiver: an analog-to-digital (A/D) board, a drop-in front-end board and a DC power distribution board. The design of the front-end and A/D boards will be discussed in this paper while the DC board will not be mentioned further, as it is simple support hardware for the receiver.



### Figure 3: Digital Backend System

### A. Analog Front-End

The receive center frequency, bandwidth and signal level are all set via a simple, replaceable front-end board. This board consists of a few surface mount components, and can easily be modified to change key radar parameters in the event use in an alternate application is desired.

### B. Digital

The digital subassembly consists primarily of an A/D converter, a de-multiplexer (DMUX) and a field programmable gate array (FPGA). The A/D is capable of directly sampling input signals up to 3.5 GHz at 10 bits utilizing bandpass sampling (at sample rates up to 2.2 GS/s). These samples are then de-multiplexed at a user-selectable rate of 1:2 or 1:4 and buffered in the FPGA. In addition to serving as a FIFO, the FPGA also behaves as a controller for the onboard Front Panel Data Port (FPDP) interface. The combination of these two functions, as well as a few other ancillary tasks, requires only a small percentage of the available FPGA resources. This oversized part enables the implementation of many application-specific, real-time functions such as digital filtering or data compression.

### C. Spaceborne Implementation

One of the primary goals in the development of the demonstration array was to maintain as flight-like a design as possible. Adhering to this principle, the requirements were derived from the spaceborne instrument scenario.

Additionally, to facilitate adaption of the receiver to a future spaceborne implementation, the three fundamental digital components within the receiver were selected based on the availability of radiation-hardened equivalents.

### III. MULTI-CHANNEL CONFIGURATION

Each receiver is capable of operating in a standalone fashion, but in order to implement the one-quarter-size demonstration array, a 16-channel configuration is required. In this arrangement, each receive element must communicate data to a central aggregator in a coordinated manner. The FPDP standard is capable of this type of multi-channel communication over the distance of approximately 1 m. As such, it serves as the perfect conduit for the demonstration array. The multi-channel data are collected on a central aggregator board and then transmitted to disc over a high-speed optical medium. The large-scale control scheme for the multi-channel configuration is shown in Figure 3. With commercial off-the-shelf hard disc drives and support hardware, the backend was designed for ease of implementation and must be modified in the eventual space-flight configuration.

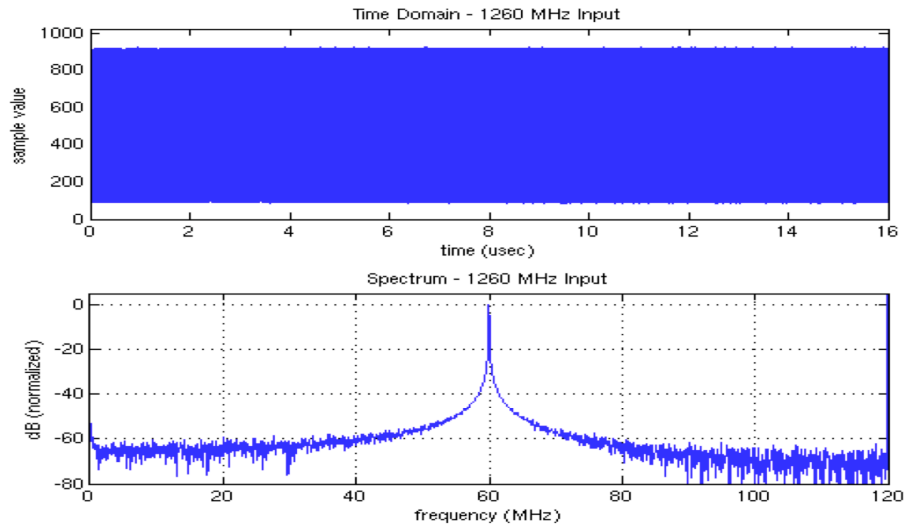


Figure 4: Sampled Data from the Prototype Receiver

#### IV. RESULTS & FUTURE WORK

The receiver development consists of two phases: prototype and demonstration unit development. Thus far, we have tested the prototype receiver in a standalone configuration. Preliminary results from this testing are shown in Figure 4. In this test case, a 1260-MHz tone was injected into the digital portion of the receiver and data were collected on a logic analyzer. The plot depicts collected samples along with an FFT of these samples depicting the frequency domain representation of the collected data. From the plot, it is clear that the spectrum is clean and the signal-to-noise ratio is approaching the ideal level for a 10-bit A/D. The data shown in Figure 5 demonstrate the low noise level inherent within the receiver. These data were collected with the input to the digital portion of the prototype receiver terminated with a 50-Ohm load.

With these promising initial results on hand, minor modifications were made to the receiver design, and the demonstration unit was fabricated. Presently we are performing initial

testing on the demonstration receiver, which is shown within a housing in Figure 2. Four of these units have been populated, and once each unit undergoes standalone checkout, multi-channel testing will commence with the demonstration data aggregation system.

#### ACKNOWLEDGEMENT

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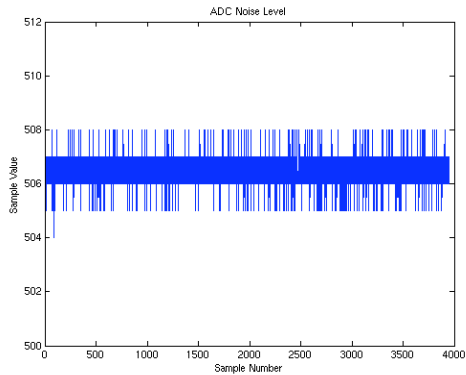


Figure 5: Noise Data from the Prototype Receiver